WHAT IS CLAIMED IS:

1. A register file comprising:
a plurality of register file cells coupled to a bit line;
a latch coupled to the bit line; and
an inverter coupled between an output of the latch and the bit line.

2. The register file as recited in claim 1, further comprising:
another inverter coupled between the bit line and an input of the latch.

3. The register file as recited in claim 1, wherein the output of the latch is an output of the register file.

4. The register file as recited in claim 1, wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter.

5. The register file as recited in claim 4, wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch.

6. The register file as recited in claim 5, wherein data is read out of the register array to be input into the latch.

7. The register file as recited in claim 1, wherein a multiplexor is not coupled between the bit line and the latch.

8. A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first tri-state inverter coupled between the first local bit line and the global bit line, the first tri-state inverter controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second tri-state inverter coupled between the second local bit line and the global bit line, the second tri-state inverter controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third tri-state inverter coupled between an output of the latch and the global bit line, the third tri-state inverter controlled by a hold signal.

9. The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

10. The register file as recited in claim 8, wherein when the third tri-state inverter is activated, the first and second local select signals are deactivated.

11. A register file comprising:

a plurality of register file cells coupled to a bit line;

a latch coupled to the bit line; and

a transmission gate circuit coupled between an output of the latch and the bit line.

12. The register file as recited in claim 11, further comprising:

an inverter coupled between the bit line and an input of the latch.

13. The register file as recited in claim 11, wherein the output of the latch is an output of the register file.

14. The register file as recited in claim 11, wherein the transmission gate circuit receives a hold select signal.

15. The register file as recited in claim 14, wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch.

16. The register file as recited in claim 15, wherein data is read out of the register array to be input into the latch.

17. The register file as recited in claim 11, wherein a multiplexor is not coupled between the bit line and the latch.

18. A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first transmission gate coupled between the first local bit line and the global bit line, the first transmission gate controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second transmission gate coupled between the second local bit line and the global bit line, the second transmission gate controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third transmission gate coupled between an output of the latch and the global bit line, the third transmission gate controlled by a hold signal.

19. The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

20. The register file as recited in claim 8, wherein when the third transmission gate is activated, the first and second local select signals are deactivated.